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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,373	02/26/2004	Tze-Hsiang Chao	SISP0011USA	2372
27765	7590	09/15/2005	EXAMINER	
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			NGUYEN, LINH M	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 09/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/708,373

Applicant(s)

CHAO, TZE-HSIANG

Examiner

Linh M. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 August 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 9-13 is/are allowed.
- 6) ☒ Claim(s) 1,3-7 and 14 is/are rejected.
- 7) ☒ Claim(s) 2,8 and 15 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

This is a reply to Applicant's amendment filed on 08/04/2005. By virtue of this amendment, claims 1-15 are currently presented in the instant application.

#### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1 and 3-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Alexander et al. (U.S. Pat. No. 6,693,473).

With respect to claim 1, Alexander et al. discloses, in Fig. 2, a multi-stage delay clock generator comprising a plurality of delay cells [52], each delay cell generating a delay signal to a subsequent delay cell in response to a delayed clock signal from a preceding delay cell and a delay control signal [78] where a first delay cell among the plurality of delay cells receives an external clock signal [72], wherein each subsequent delay cell comprises a smaller delay step than the current delay cell (*i.e. first delay cell includes 5 inverters, second delay cell includes 4 inverters, third delay cell includes 3 inverters from delay line 52*); a phase detector [56],

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responsive to the external clock signal [72] and a feedback clock signal [74], for generating a lock control signal [comp]; and a control unit, responsive to the lock control signal, for generating the delay control signal for programming the delay cells.

With respect to claim 3, Alexander et al. discloses, in Fig. 2, that a range of the first delay cell is greater than a range of a maximum delay target from the external clock signal [72].

With respect to claim 4, Alexander et al. discloses, in Fig. 2, that the delay step of a last delay cell is smaller than a system jitter.

With respect to claim 5, Alexander et al. discloses, in Fig. 2, that a delay step of the first delay cell is determined by a total number of programming bits.

With respect to claim 6, Alexander et al. discloses, in Fig. 2, that the total number of programming bits is a value from dividing the range of the maximum delay target by the delay step of the first delay cell.

With respect to claim 7, Alexander et al. discloses, in Fig. 2, that a number of delay cells is dependent on a resolution of the last delay cell.

3. Claim 14 is rejected under 35 U.S.C. 102(e) as being anticipated by Okayasu (U.S. Pat. No. 6,549,052).

With respect to claim 14, Okayasu discloses, in Fig. 7, a multi-stage delay clock generator for generating a delay signal, comprising: a first delay chain [26a] for generating a first delay signal, in response to an external clock signal [reference clock] and a first delay control signal [output from 24a], comprising a plurality of delay cells [28], each delay cell generating a delayed clock signal to a subsequent delay cell in response to a delayed clock signal from a preceding delay cell and a delay control signal, wherein each subsequent delay cell comprises a

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smaller delay step than the current delay cell (*i.e. first delay cell includes 5 inverters/buffers, second delay cell includes 4 inverters/buffers, third delay cell includes 3 inverters/buffers from delay line 26a*); a second delay chain [26b] for generating a second delay signal, in response to a second delay control signal [output from 24b] and a feedback clock signal [output from 26b], comprising a plurality of delay cells, each delay cell generating a delayed clock signal to a Subsequent delay cell in response to a delayed clock signal from a preceding delay cell and a delay control signal, wherein each subsequent delay cell comprises a smaller delay step than the current delay cell (*i.e. first delay cell includes 5 inverters/buffers, second delay cell includes 4 inverters/buffers, third delay cell includes 3 inverters/buffers from delay line 26b*); a first phase detector [22a], responsive to a delayed external clock signal and the first delay signal, for generating a first control signal [output of 22a]; a second phase detector [22b], responsive to a delayed feedback clock signal and the second delay signal, for generating a second control signal [output of 22b], a control unit [24a, 24b], responsive to the first [output of 22a] and the second control signal [output of 22b], for generating the first delay control signal and the second delay control signal, and a control unit for programming the delay cells.

***Allowable subject matter***

4. Claims 9- 13 are allowed.
5. Claims 2, 8 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
6. The following is a statement of reasons for the indication of allowable subject matter:  
  
The closest prior art of record does not show or fairly suggest:

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a) A multi-stage delay clock generator, in which the control unit comprises a delay counter, responsive to the lock control signal, for generating the delay control signal, a plurality of multiplexers, responsive to the delay control signal, for outputting a select signal, and a plurality of latches, responsive to the select signal, for outputting a lock signal to the plurality of delay cells and to a subsequent multiplexer, as called for in claim 2;

b) The multi-stage delay clock generator further comprises a delay offset electrically coupled to a last delay cell for generating an offset delay signal, as called for in claim 8;

c) A method for generating a delay signal with a step of latching the delay cell according to the lock control signal, in combination with the remaining claimed limitations, as called for in claim 9; and

d) A multi-stage delay clock generator, in which the control unit includes a delay counter, responsive to a lock control signal, for generating the delay control signal, a plurality of multiplexers, responsive to the delay control signal, for outputting a select signal; and a plurality of latches, responsive to the select signal, for outputting a lock signal to the plurality of delay cells and to a subsequent multiplexer, as called for in claim 15.

***Remarks***

7. Applicant's response filed 08/04/2005 has been seriously considered; however, previously stated allowable subject matters have been withdrawn due to newly discovered prior art to Alexander et al. and Okayasu as set forth in the office action.

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***Inquiry***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN



**LINH MY NGUYEN  
PRIMARY EXAMINER**